

Multiplierless Approximate 4-point DCT VLSI Architectures for Transform Block Coding

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Abstract

Two multiplierless algorithms are proposed for 4×4 approximate-DCT for transform coding in digital video. Computational architectures for 1-D/2-D realisations are implemented using Xilinx FPGA devices. CMOS synthesis at the 45 nm node indicate real-time operation at 1 GHz yielding 4×4 block rates of 125 MHz at less than 120 mW of dynamic power consumption.

1 Introduction

Video and multimedia processing based on signal and image compression such as the high efficiency video coding (HEVC) and H.265 reconfigurable video codecs require 2-D transform block coding for block sizes $N \times N$ where $N \in \{4, 8, 16, 32, 64\}$ [1]. The transform coding stage requires algorithms for the N -point discrete cosine transform (DCT) of types II and IV. The associate transformation matrices are defined, respectively, according to [2]:

$$[\mathbf{C}_{II}]_{(m,n)} = \sqrt{\frac{2}{N}} \cdot \alpha_m \cdot \cos \left[\left(m - \frac{1}{2} \right) \cdot \frac{\pi(n-1)}{N} \right],$$

$$[\mathbf{C}_{IV}]_{(m,n)} = \sqrt{\frac{2}{N}} \cdot \cos \left[\left(m - \frac{1}{2} \right) \cdot \left(n - \frac{1}{2} \right) \cdot \frac{\pi}{N} \right],$$

where $m, n = 1, 2, \dots, N$, $\alpha_1 = 1/\sqrt{2}$, and $\alpha_m = 1$, for $m > 1$.

In this letter, our goal is to propose multiplication-free approximations for the 4-point DCT-II and -IV as well as its fast algorithms. We also aim at VLSI realisations of both 1-D and 2-D versions of the derived approximate transforms, while maintaining at high numerical accuracy and low computational complexity.

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2 Optimisation and orthogonalization

Let $\mathcal{M}_P(4)$ be the set of all 4×4 matrices whose entries are defined over $P = \{-1, 0, 1\}$. In this set, all matrices represent multiplierless transformations. Our goal is to find matrices in $\mathcal{M}_P(4)$ that satisfactorily approximate \mathbf{C}_{II} and \mathbf{C}_{IV} .

Therefore we propose the following multivariate non-linear optimisation problem over $\mathcal{M}_P(4)$

$$\mathbf{C}_k^* = \arg \min_{\mathbf{A} \in \mathcal{M}_P(4)} \text{error}(\mathbf{A}, \mathbf{C}_k), \quad k \in \{\text{II}, \text{IV}\}, \quad (1)$$

where \mathbf{C}_k^* are the optimal matrices and $\text{error}(\cdot, \cdot)$ is an error measure between a given candidate matrix and the exact matrices \mathbf{C}_{II} and \mathbf{C}_{IV} .

Let $h_i[n]$ be the discrete signal formed by the i th row of a given matrix \mathbf{T} and the discrete-time Fourier transform (DTFT) of $h_i[n]$ be denoted by $H_i(\omega; \mathbf{T})$. As discussed in [3,4], we adopted the total error energy as the error measure. This particular measure is defined as follows:

$$\varepsilon(\mathbf{A}, \mathbf{C}_k) = \sum_{m=1}^4 \int_0^\pi |H_m(\omega; \mathbf{A}) - H_m(\omega; \mathbf{C}_k)|^2 d\omega,$$

for $k \in \{\text{II}, \text{IV}\}$. In other words, $\varepsilon(\mathbf{A}, \mathbf{C}_k)$ quantifies the sum of the energy error in the DTFT domain—between \mathbf{A} and \mathbf{C}_k —when the entries of a given matrix row are interpreted as filter coefficients [3,4]. This quantity can be computed numerically by standard quadrature methods [5].

As an additional constraint to (1), we impose that the matrix $\mathbf{A} \cdot \mathbf{A}^\top$ must be a diagonal matrix to ensure that orthogonality can be achieved in the obtained approximations [6]. The resulting constrained optimisation problem is algebraically intractable and we resorted to exhaustive computational search.

3 Proposed 4-point DCT approximations

By solving (1), we obtained the following new DCT approximations:

$$\mathbf{C}_{\text{II}}^* = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 0 & 0 & -1 \\ 1 & -1 & -1 & 1 \\ 0 & -1 & 1 & 0 \end{bmatrix} \quad \text{and} \quad \mathbf{C}_{\text{IV}}^* = \begin{bmatrix} 1 & 1 & 1 & 0 \\ 1 & 0 & -1 & -1 \\ 1 & -1 & 0 & 1 \\ 0 & -1 & 1 & -1 \end{bmatrix}.$$

Although possessing very low complexity, these matrices are not orthogonal. In several contexts, such as image processing for coding, orthogonality is often a desirable property [2]. Adopting the orthogonalization methods detailed in [6], new orthogonal matrices $\hat{\mathbf{C}}_{\text{II}}$ and $\hat{\mathbf{C}}_{\text{IV}}$ can be derived based on \mathbf{C}_{II}^* and \mathbf{C}_{IV}^* , respectively. These orthogonal

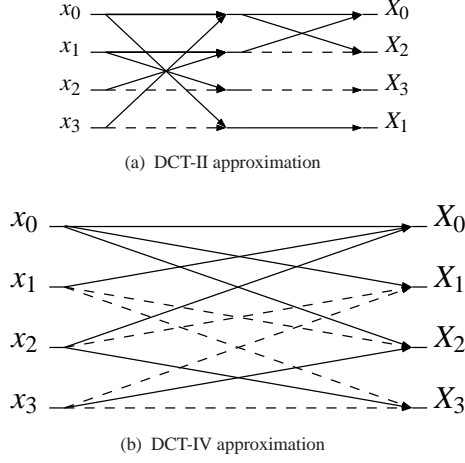


Figure 1: Signal flow graph for proposed transforms.

matrices are given by:

$$\hat{\mathbf{C}}_{\text{II}} = \mathbf{D}_{\text{II}} \cdot \mathbf{C}_{\text{II}}^* \quad \text{and} \quad \hat{\mathbf{C}}_{\text{IV}} = \mathbf{D}_{\text{IV}} \cdot \mathbf{C}_{\text{IV}}^*,$$

where $\mathbf{D}_{\text{II}} = \sqrt{[\mathbf{C}_{\text{II}}^* \cdot (\mathbf{C}_{\text{II}}^*)^\top]^{-1}}$ and $\mathbf{D}_{\text{IV}} = \sqrt{[\mathbf{C}_{\text{IV}}^* \cdot (\mathbf{C}_{\text{IV}}^*)^\top]^{-1}}$. Explicitly we obtain that

$$\mathbf{D}_{\text{II}} = \text{diag} \left(\frac{1}{2}, \frac{1}{\sqrt{2}}, \frac{1}{2}, \frac{1}{\sqrt{2}} \right)$$

and

$$\mathbf{D}_{\text{IV}} = \frac{1}{\sqrt{3}} \cdot \mathbf{I}_4,$$

where \mathbf{I}_4 is the identity matrix of size 4. In image compression context the scaling matrices \mathbf{D}_1 and \mathbf{D}_2 may not introduce any computational overhead, because they can be merged into the quantisation step, as described earlier in [4, 7–9].

The signal flow graph for \mathbf{C}_{II}^* and \mathbf{C}_{IV}^* is shown in Fig. 1. We note that the \mathbf{C}_{II}^* and \mathbf{C}_{IV}^* transformations require only 6 and 8 additions, respectively. Multiplications or bit-shifting operations are totally absent. Resulting approximations $\hat{\mathbf{C}}_{\text{II}}$ and $\hat{\mathbf{C}}_{\text{IV}}$ are very close to the respective ideal DCT and offer extremely low complexities. In Table 1, we show the error measure and arithmetic complexity for the proposed transforms, the exact DCT computation [2], and the well-known signed DCT [3].

Table 1: Total error energy and arithmetic complexity analysis

Method	Error Energy	Complexity		
		Add.	Mult.	Total
Exact 4-point DCT-II [2]	0.000	8	4	12
4-point Signed DCT-II [3]	0.957	8	0	8
Proposed $\hat{\mathbf{C}}_{\text{II}}$	0.957	6	0	6
Exact 4-point DCT-IV [2]	0.000	12	8	20
4-point Signed DCT-IV [3]	2.359	10	0	10
Proposed $\hat{\mathbf{C}}_{\text{IV}}$	0.838	8	0	8

Table 2: Resource consumption on Xilinx XC6VSX475T-2FF1156

Proposed Approx.	CLB	FF	LUT	Slices	F_{max} (MHz)	D_p (W)
1-D DCT-II	56	76	92	35	743.5	0.535
1-D DCT-IV	76	132	128	52	735.3	0.574
2-D DCT-II	166	408	330	108	704.2	0.884
2-D DCT-IV	210	528	472	148	689.2	0.921

4 FPGA prototypes

The approximate DCTs were realised as an architecture for the 4-point 1-D transforms and the extended to 4×4 2-D transformation. The inputs were assumed at 8-bit resolution. Rapid prototypes were realised on a Xilinx Virtex-6 field programmable gate array (FPGA) device and tested to ensure correct on-chip functionality. The results concerning the consumption of configurable logic blocks (CLB), flip-flops (FF), look-up tables (LUT), and slices are shown in Table 2. The maximum operating frequency (F_{max}) and dynamic power consumption (D_p) are also displayed.

The register transfer language (RTL) code corresponding to the FPGA-verified designs were targeted to 45 nm CMOS standard cell process using Cadence Encounter. The CMOS designs were realised up to synthesis and place-and-route levels leading to the estimated results in Table 3. Area-time complexities AT and AT^2 were adopted and measured in $\mu\text{m}^2 \cdot \text{ns}$ and $\mu\text{m}^2 \cdot \text{ns}^2$, respectively.

Table 3: Resource consumption for 45 nm CMOS

Proposed Approx.	ASIC Gates	Area (μm^2)	F_{max} (GHz)	D_p (mW)	AT	AT^2
1-D DCT-II	849	3386.9	1.10	6.31	3160	2948
1-D DCT-IV	1207	4870.4	1.00	8.62	4846	4822
2-D DCT-II	7400	31217.8	0.95	59.33	7770	8159
2-D DCT-IV	13770	59052.5	0.94	115.66	14596	15472

5 Conclusion

Numerical optimisation methods have lead to 4-point approximations for the DCT-II and DCT-IV. Such matrices are tailored for minimal computational complexity and are adequate for computing realisations linked to coding operations with applications in digital video and multimedia. Fast algorithms were derived and the associate physical realisations do not require VLSI area- and power-intensive multiplier circuits. Both 1-D and 2-D realisations were proposed with FPGA prototypes for architecture validation and CMOS synthesis results at the 45 nm node. Results indicate real-time blockrate of 125 MHz for processing 4×4 blocks at 1 GHz clock frequency.

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